Original Research Article

# Application of square P + structures in silicon carbide JBS

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***Abstract:*** In this study, the structure of P + doping zone of silicon carbon (SiC) (junction barrier Schottky diode, JBS). The above two SiC JBS structures were tested, and the forward and backward characteristics were analyzed and compared. As a result, the square structure is 17.67% less resistant than the bar structure. In short, bar diodes perform better in reverse ability, while square diodes have more advantages in positive guide ability. The results provide an important basis for the optimized design and application of silicon carbide devices.

***Keywords:*** Silicon carbide; JBS; Forward and negative direction characteristics

## 1. Introduction

### 1.1. Research background and significance

With the rapid development of semiconductor technology, SiC, as a high-performance semiconductor material, has attracted much attention for its excellent electrical, thermal and mechanical properties. SiC Materials show excellent stability in extreme environments such as high temperature, high frequency and high power, making them have a wide application prospect in power electronics, aerospace, automobile manufacturing and other fields [1,2]. Therefore, the comparative study of the properties of different structures in the active region of silicon carbide can not only help to deeply understand the performance characteristics of SiC materials, but also provide important theoretical support and experimental basis for the optimal design and application of silicon carbide devices.

In recent years, with the rapid development of new energy vehicles, smart grid and other fields, the demand for high-performance power electronic devices is increasing. Carbon SiC material has become an ideal material[3,4] for manufacturing high-performance power electronic devices because of its excellent properties such as high breakdown electric field, high thermal conductivity and low dielectric constant. However, the properties of silicon carbide materials are affected by various factors such as its structure and preparation process. Therefore, this study aims to explore the influence mechanism of different structures on the properties of SiC materials by comparing the properties of the square structure, so as to provide a scientific basis for the optimal design and application of SiC devices.

### 1.2. SiC JBS introduction

SiC JBS Is a high voltage resistant, high speed rectifier, it combines the excellent performance of SiC materials, providing excellent performance for modern power electronics applications[5-7]. SiC JBS Compared with traditional Si diode devices, it has higher voltage resistance, lower leakage and excellent reverse recovery characteristics of “zero”, which enables SiC JBS devices to operate at higher working frequency and work stably in higher temperature environment.

The main structural feature of the SiC JBS device is the integration of multiple PN junctions in the drift region of the ordinary SiC Schottky diode, forming a composite rectifying structure. At the forward bias voltage, the Schottky diode directs on first, and with the increase of the reverse bias voltage, the PN junction diode also starts to turn on, and the conductance modulation effect further reduces the positive guide voltage drop of the SiC JBS device. At the reverse bias voltage, the depletion zone formed by the PN junction expands to the channel region, forming a barrier that effectively suppresses the Schottky barrier reduction effect and greatly reduces the reverse leakage current by [8,9].

SiC JBS The performance advantages of devices include high current density, high working junction temperature, low switching loss, high efficiency, high power density and higher frequency applications. These advantages make SiC JBS devices have a wide application prospects in new energy vehicles, charging piles, photovoltaic inverter, high-end power supply and other application fields.

In general, SiC JBS devices, as an advanced power electronics device, with excellent performance and wide application prospects, are an indispensable part of the modern power electronics field.

### 1.3. Research purpose and problem elaboration

With the rapid development of semiconductor technology, SiC, as a high-performance semiconductor material, attracts much attention due to its excellent electrical, thermal and mechanical properties. The purpose of this study is to deeply explore the differences in the performance between the bar structure and the square structure of SiC active region, in order to provide theoretical support and practical guidance for the application of SiC materials in power electronics, high temperature devices and other fields. Specifically, this research will revolve around the SiC active area of structure design, preparation process, performance evaluation and influencing factors, through comparative analysis of the bar structure and square structure in the electrical performance, thermal and mechanical performance differences, reveals the mechanism of the performance, and discusses the key factors affecting the performance.

## 2. Design and preparation of the structures

### 2.1. Exaxial design principles and parameters

SiC JBS Diode and other power devices in the reverse working state, the reverse voltage is mainly carried by the epitaxial layer. Specifically, the larger the thickness of the epitaxial layer and the lower the doping concentration, the higher the reverse voltage that the device can withstand. However, this is accompanied by a corresponding increase in the on resistance. On the contrary, if the voltage resistance of the device is low, its conduction resistance will be relatively small. Therefore, in the design and manufacturing process, the thickness and doping concentration of the epitaxial layer need to be carefully selected to ensure that the device has a high reverse breakdown voltage and reduce the conduction resistance as much as possible, so as to reduce the energy loss and improve the overall performance of the device.

Generally, the punch through, PT) device structure is selected to design the thickness of the epitaxial layer. The critical breakdown can be expressed as:

$$E(x) = E_C - \frac{qN_d}{\varepsilon_s} x, x \le t_{epi}$$

Where E (x) is the electric field distribution function, $E_C$For the critical breakdown field strength, q is the charge of the electron, $N_d$Is the doping concentration of the epitaxial layer, is the dielectric constant of 4H-SiC, x is the epitaxial layer depth, $t\varepsilon s_{epi}$Is the epitaxial layer thickness.

According to the empirical formula [10] for the critical breakdown field strength of 4H-SiC materials at room temperature provided by Konstantinov et al

$$E_C \approx \frac{2.49\times 10^6}{1-0.25log_{10}\left(\frac{Nd}{10^6}\right)}$$

The breakdown voltage V of the device$_{BR}$The relation with the electric field is as follows:

$$V_{BR} = \int_0^{t_{epi}} E(x)dx = E_C t_{epi} - \frac{qN_d t_{epi}^{\ \ 2}}{2\varepsilon_S}$$

The conduction-on resistance of the device drift zone is as follows

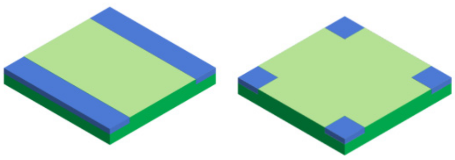
$$R_{\mathrm{on},sp} = \frac{t_{epi}}{q\mu_n N_d} = \frac{4V_{BR}^2}{\mu_n \varepsilon_S E_C^3}$$

among, $\mu_n$Represents the mobility of 4H-SiC.

Combined with the upper formula, according to the design target of the JBS device breakdown voltage of 1200$V_d$=8×$10^{15}$cm-3, $t_{epi}$=10μm.

## 2.2. Design of the active area

The square cell structure of SiC JBS (junction barrier Schottky diode) in the active region is significantly different from the traditional bar cell structure. First of all, silicon carbide JBS active area square cell structure is designed to meet the demand of specific high performance, it can have a greater proportion of Schottky contact area, so the guide resistance will decrease, conduction loss will decrease, make full use of P + area and N extension depletion area, to shield the high electric field on Schottky contact. Therefore, the same device area square cell structure performance is better than the bar device structure. The schematic representation of its cellular 3D structure is shown in Figure 1.



(a) (b)

**Figure 1. 3D schematic diagram of the cell structure injected into the source area. (a) schematic diagram of the injection of the cell structure with a strip-shaped source area, (b) schematic diagram of the injection of the cell structure with a square-shaped source area.**

At present, all chip manufacturers still use the bar cell shown in Figure 1 (a) rather than the square cell structure shown in Figure 1 (b). The main reason is that the pressure resistance effect of the square cell is worse than that of the bar cell.

In this paper, we mainly designed and manufactured a square cell device, in which the resistance of the same area decreases by 17.67% compared with the bar cell, the output of the same forward characteristic device increases by 20%, and the reverse voltage characteristic can still meet the current needs of the industry.

After simulation analysis, the cell structure is set as: bar injection structure p + injection 1.5 um, 2.5 um interval; square injection structure p + injection side is 1.5 um long, 2.5 um interval.

### 2.3. Preparation process and preparation process

The preparation process of semiconductor power devices involves multiple well-designed steps to ensure the high performance and reliability of the final product. First, the silicon carbide wafer is cleaned first to ensure that the surface is clean. The mask technology is then used to transfer the graphic pattern needed for chip making to the silicon carbide wafer, a step taken by selecting the appropriate light source and mask for exposure, and then the pattern appears on the silicon wafer by development.

Ion injection is the core step in the semiconductor process, which is used to adjust the electronic properties of semiconductor materials and realize the specific electrical properties of devices. In the process of ion injection, it is necessary to choose the appropriate doping material and energy according to the silicon carbide wafer. Diffusion is the key step to make the distribution of doped materials uniform. The doped material is diffused to the inside of the silicon carbide wafer through high temperature treatment, and then sintering treatment to strengthen the connection between the doped material and the silicon wafer.

Metalization is a key step in making a semiconductor device into a conductive path, involving sputtering the metal on the surface of the silicon wafer and then removing the unwanted metal parts to form the metal line of the conductive path.

After metallization, the chip is sliced, dividing a complete silicon wafer into several small chip fragments. This step requires precise division to ensure that each chip meets the design requirements and can be used independently.

Finally, packaging is the step of connecting the chip to the wire and sealing it inside one housing. During the packaging process, the electrical performance and connection of the chip will be tested to ensure that the chip works properly. After passing the test, the chip is packaged to complete the whole preparation process of the semiconductor power device.

## 3. Performance comparison of 3-bar structures and square structures

The electrical characteristic data of the samples used KEYSIGHTs B1505A power device analyzer and N1265A module, and were tested and collected with the semi-automatic probe table. The Kelvin test method was used to accurately test the samples.

### 3.1. Positive wizard feature

The test conditions of the two devices are: 0-10V step voltage, current limit of 25A.

The test results of the device are shown in Figure 2, and the conduction voltage drop of the bar and square P + zone diode at 20A is 1.3194V and 1.2395V, respectively. This rate was reduced by 5.92%. In the positive guide feature, the resistance bar in the conduction state is 17.70m Ω, the square resistance is 14.53m Ω, and the square structure is 17.67% lower than the bar structure.

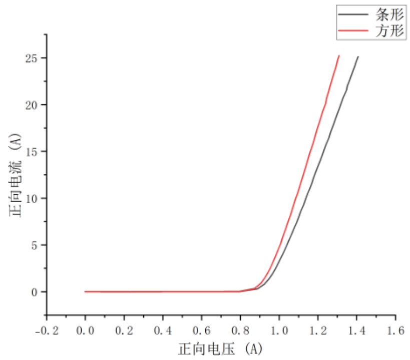
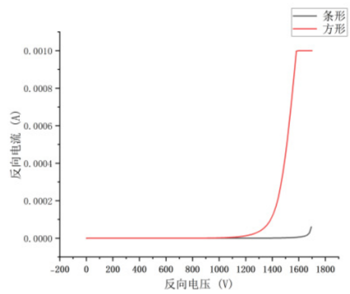



**Figure 2. Forward I-V curve diagram.**

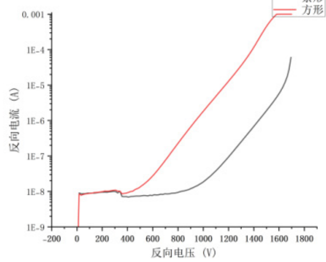
## 3.2. Reverse breakdown feature

The test conditions of the two devices are: 0-1700V step voltage, current limit of 1 mA.

The test results are shown in Figure 3, in the reverse blocking state, the current around 1E-8 A should be the minimum accuracy of the test current of the test equipment. When the voltage is greater than 400V, the leakage current of the square structure increases significantly, which is larger than that of the bar structure. When the current reaches 1 mA, the voltage of the square structure is 1598V, and the bar structure is greater than 1700V. When the reverse voltage reaches 1200V, the leakage of the square structure reaches 13.06 μ A, and the leakage current of the bar structure is 94.51nA. Although the leakage current of the square structure is 139 times higher than that of the bar structure, there is no breakdown trace of the square structure, and the leakage current is caused by the large tunneling current. Under the industry standard 200 μ A condition, it also reached 1445V, far exceeding the 1200V standard.




(a)




(b)

**Figure 3. Reverse characteristic curve diagram. (a) reverse I-V curve diagram, (b) everse $log_{10}$I-V curve diagram.**

## 4. Discussion

Combined with the above test parameters, the square structure is more advantageous than the bar structure.

In JBS diode in reverse bias, the depletion area increases, conductive channel is broken, reverse voltage is mainly borne by the PN junction, in the process of flow because two graphic structure is in the same wafer two structure using the same erosion process conditions, the process conditions will make different window area erosion rate is different, the window area smaller erosion rate is slower, so the actual square P + area will be smaller than the design.

Also, as shown in Figure 4, in the diagonally oriented P + region at a distance of $W_{P+2}$Will compare with the correct P + zone $W_{P+1}$The distance, which will lead to the weak depletion area at the intersection of the conductive channel clamping is slower than the bar, the two sides have been broken, and the central point is not broken, which leads to the large leakage.

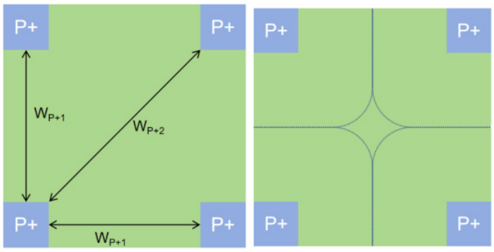



**Figure 4. Schematic diagram of the cells top-view structure. (a) Schematic diagram of the distance between each P+ region, (b) Schematic diagram of the depletion region of the PN junction.**

The optimized direction can align the P + area structure width and place the P + region in the vertex position of the positive triangle. Or placed with a regular hexagonal P + area, the distance of the P + area can be designed to be an equal distance, as shown in Figure 5.

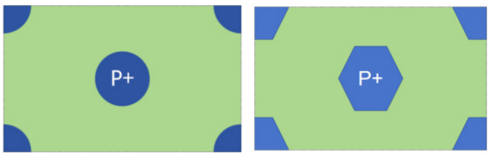



**Figure 5. The schematic diagram of placing the cell at the vertex position of the positive triangle in the P+ area.**

## 5. Conclusion

After a thorough comparison of the strip structure and the square structure of the silicon carbide active region, we draw a significant conclusion, but also realize the insufficiency. In terms of electrical performance, the bar structure shows a good reverse ability, especially in terms of reverse leakage current. The square structure, because of the large Schottky contact area, shows a good positive guide ability.

Next, it will be further investigated to design the structural distance of the P + region to a consistent width to investigate whether the reverse characteristics can make full use of the depletion region brought by the P + region to achieve a small reverse leakage current.

This research conclusion not only provides an important reference basis for the application of silicon carbide materials, but also points out the direction for the research and development of silicon carbide materials in the future.

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