Original Research Article

Studies on the structure of the U-groove vdmosfet devices

Yili Xu[1][*Corresponding Author], *Xin Li* [1], *Xiaodong Yin*[1], *Guowei Zhang*[1], *Jingyi LI*[1], *Qianqian Liu*[2]

1 Hangzhou Spectrum Semiconductor Co., Ltd., Hangzhou Xiaoshan, 310000, China
2 Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, 100029, China

Abstract: Power semiconductor devices are very important in modern power electronics technology, especially in the field of low power consumption and high efficiency. With the development of technology, the demand for high-voltage, high-frequency and high-efficiency semiconductor devices is growing, which provides support for the development of new energy, smart grid, energy storage, automotive and other fields. At present, the power devices on the market mainly use the VDMOSFET and UMOSFET two structures. UMOSFET Due to the difficulty of manufacturing the U slot, many manufacturers abandon development and optimize VDMOSFET instead. The development and optimization of silicon carbide VDMOSFET mainly focuses on improving the device performance. This paper proposes a new method of source U groove VDMOSFET structure, by increasing in the original manufacturing process of the U groove etching, different from UMOSFET morphology of the U groove, greatly reduces the U groove erosion difficulty, and sub-trench defects do not affect the final performance of the device, and can reduce the cell size of the device, improve the current density, provide new ideas for device development.

Keywords: Silicon carbide; Diode; Terminal structure

1. Introduction

Power semiconductor devices play an important role in modern power electronics technology, especially in the field of low power consumption and high efficiency[1]. With the rapid development of power electronics technology, the global demand for high voltage, high frequency and high efficiency semiconductor devices is increasing day by day, providing an important guarantee for the development of new energy, smart grid, energy storage, automobile and other fields[2-4]. At present, most MOSFET structures in the power device industry are VDMOSFET and UMOSFET. UMOSFET In the development of products, we need to ensure that the two sides of the U groove are parallel and cannot form sub-trench, which is difficult in etching[5]Therefore, many power device manufacturers have to give up the development of UMOSFET products and put research and development energy into VDMOSFET development and optimization. The schematic diagram of the cell structures of the existing VDMOSFET devices is shown in **Figure 1.**

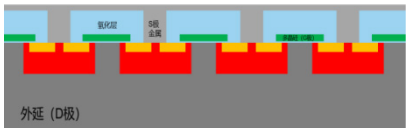

Figure 1. Schematic diagram of the cell structure of the existing VDMOSFET devices.

The development and optimization of silicon carbide VDMOSFET are mainly reflected in the improvement of device performance, including mobility, reliability, switching loss, threshold voltage, blocking voltage and on resistance, etc.

Starting with the cell structure of the device, we invented a U slot VDMOFET device to introduced the

VDMOSFET device to reduce the size of the cell and increase the current density of the device, which provides a new idea for the continuous development of the device.

2. The sic vdmosfet structure in the international market

The cell size of the existing VDMOSFET devices available internationally is around 9um[6-8], Its cell dimensions is roughly shown in Figure 2

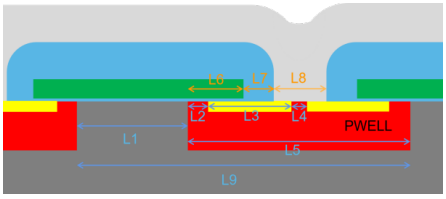

Figure 2. Schematic diagram of vdmosfet cells being sold in the current international market.

As shown in Figure 2, the cell size L9 is about 9um; L1 is the width of JFET area. In the current international device design, JFET area is usually injected, and the single cell resistance of the device can be roughly expressed as $R_{dson}=R_s+R_{ohm(s)}+R_{N+}+R_{ch}+R_{JFET}+R_{epi}+R_{sub}+R_{ohm(D)}+R_D$, among,$R_{JFET}$ Represents the JFET zone resistance, Injection of the JFET region can reduce the JFET zone resistance, The design width of the JFET area after injection is generally L1=2um; L2 is the channel length of the device, Devices in the current international market, The length of the channel is generally L2=0.5um; L3 for the N + injection width, Generally limited by the width of L6, L7, L8; L4 for the P + injection width, Generally limited by the source-pole ohmic contact during device design, Generally, L4=1um; L5 for the PWELL injection width, L5=2L2 + 2L3 + L4; L6 is limited by the channel length L2 and the coverage length of the N + region, Generally, L6=1.5um; L7 is the width of the gate source, Generally has the same thickness as the gate source isolation oxide layer, Limited by the quality of the isolated oxide layer, Generally, L7=1um; L8 is the source pole ohmic contact width, The source metal of the device must be kept in contact with PWELL and N +, In order to maintain the potential of PWELL with N + to 0, Generally, L8=2um; as what mentioned before, L9=L1+L5=L1+2L2+2L3+L4=L1+2L6+2L7+L8= 9um.

As mentioned above, the cell size of SiC VDMOSFET devices has been difficult to decrease due to the limitations of various materials and electrical parameters. It is difficult to continue to reduce the cell size will cause the current density of the device to continue to increase, and then lead to the area of the same conduction resistance device is difficult to continue to decrease. No more smaller device area means no more lower device manufacturing costs, a result that no chipmaker would want to see.

3. The U-groove vdmosfet structure

3.1. Size advantage of the u-slot vdmosfet structure

A U groove VDMOSFET structure is presented, whose schematic diagram is shown in Figure 3

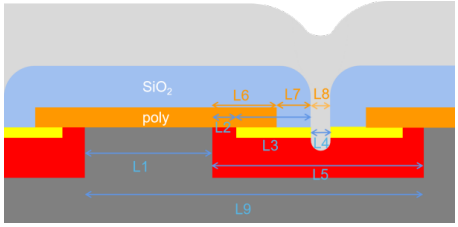

Figure 3. Schematic structure of U groove vdmosfet.

Compared with the conventional VDMOSFET, the U groove VDMOSFET changes the source ohmic contact from transverse to longitudinal, and changes the necessary width for the Ohm contact to the U groove depth, reducing the device cell size. U slot VDMOSFET reduces the size limit of the design end to ohmic contact, and reduces the size limit of the N + area. The width of L4 begins to be limited by the lithography size and etching ability, so the size of L4 can still be further reduced.

As shown in Figure 3, the cell length of U groove VDMOSFET is L9=L1 + 2L2 + 2L3 + L4=L1 + 2L6 + 2L7 + L8, where L8=L4 has the same design and material restriction conditions, and the structural cell size in **Figure 3** is L9=2um+2*1.5um+2 * 1um + 1um=8um.

3.2. Manufacturing process and process of u-groove

The manufacturing method and process of U groove VDMOSFET are as follows:

1. According to the injection area of VDMOSFET devices in normal VDMOSFET devices, the basic injection morphology is formed in the epitaxial layer;

Figure 4. Post-injection of VDMOSFET devices.

2. Gluding, exposure, development, glue, glue, block the area outside the U slot;

Figure 5. Schematic diagram after lithography process.

3. Dry etching to form U groove, N-SOURCE area through, glue;

Figure 6. Schematic diagram after dry etching and resist stripping.

4. Grid oxygen oxidation, the formation of gate oxygen layer, deposition of polysilicon, lithography, etching polysilicon, etching oxide layer;

Figure 7. Schematic diagram after gate oxidation and deposition of polycrystalline silicon etching is completed.

5. Deposit oxide layer, lithography, dry etching oxide layer, forming an isolation layer;

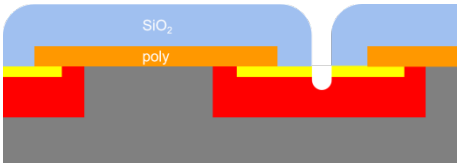

Figure 8. Schematic diagram of deposited oxide isolation layer and after etching.

6. Deposit ohm contact the metal and anneal, continue the subsequent process until the device is completed

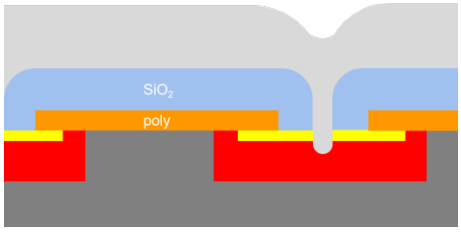

Figure 9. Schematic of Ohmic contact fabrication with deposited metal and thick metal layer afterwards.

As in the above process step, the U groove etching in step 3 is the process processing difficulty of each manufacturer, mainly because it is difficult to avoid the emergence of sub-trench during the U groove etching, as shown in FIG. 10.

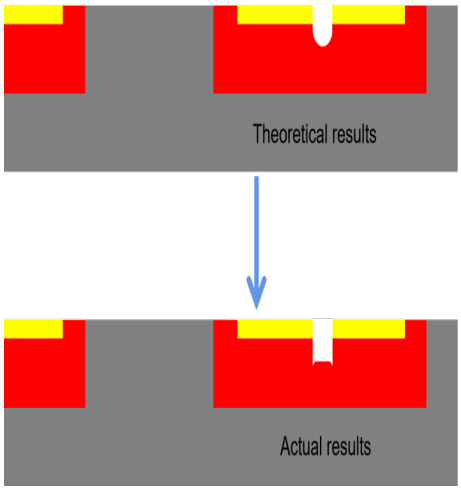

Figure 10. Sub-trench schematic diagram.

In Figure 10, the emergence of sub-trench is also one of the important reasons for most chip manufacturers to abandon UMOSFET. The U groove VDMOSFET described in this paper is different from UMOSFET with different U groove etching requirements. The presence or absence of sub-trench in step 3 does not affect the performance of the device, this is because the U groove of the structure is mainly used to form ohmic contact, and the formation of the alloy between metal and silicon carbide, the alloy layer in one direction, and various angles become smooth, as shown in Figure 11.

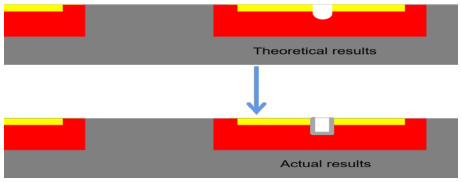

Figure 11. Schematic diagram of the alloy rear u-groove.

4. Conclusion

The U-slot VDMOSFET has the following advantages and benefits over the existing VDMOSFET:

1、The production method of U groove VDMOSFET structure is simple, only add a U groove etching in the original manufacturing process;

2、The U groove VDMOSFET structure has low requirements for the U groove etching, which can cause parallel defects in the left and right sides of the U groove and the bottom corner sub-trench, which does not affect

the final performance of the device;

3、The U groove VDMOSFET structure has a smaller single cell size than the traditional VDMOSFET structure.

In conclusion, the U-groove VDMOSFET structure has a larger current density compared with the conventional VDMOSFET structure with the same device size. Moreover, with the progress of the device process and the optimization of the design, the material limiting factor in the ordinary VDMOSFET cell structure will inevitably decrease, which will reduce the isolation layer thickness L7, the JFET area width L1 and the length of L6 in Figure 2, thus reducing the cell size L9. The U groove VDMOSFET described in this paper will not be able to reduce the cell size through material optimization and design optimization. In the case of the limit performance of each material, the cell size is forcibly reduced by more than 1um, and the structural advantage is more obvious when the smaller the cell size, which is of guiding significance for the development of silicon carbide MOSFET.

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