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Original Research Article

Research and implementation of multi-channel arbitrary wave signal synchronous measurement technology

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Abstract: In this study, a high-voltage pulse generator and a multifunctional waveform generator based on lateral heterojunction structure are designed to meet the requirements of fast switching and frequency domain correction in high-frequency signal processing of wide-band gap semiconductors. The system adopts N-type β-gallium oxide /p-type silicon carbide lateral heterojunction device, which realizes ultra-high-speed switching under the peak voltage of 800V and has the characteristics of low on-resistance. The digital programmable gate drive module based on PLL synchronization dynamically adjusts polynomial coefficients through FPGA to compensate the nonlinear transmission deviation of transistors; The measuring unit combines high-speed ADC and Wiener filtering algorithm to correct amplitude-frequency distortion in 10GHz bandwidth and ensure waveform synthesis accuracy. The system integrates Jacobian matrix control strategy and active voltage clamping technology, and connects the traditional module structure in series to maintain the dynamic stability of high-speed conversion. The two-dimensional electron gas channel formed by heterojunction polarization effect significantly optimizes the switching performance, which is verified by synchronous pulse excitation mechanism and real-time DSP analysis. The scalable waveform generation scheme proposed in this paper provides accurate waveform support for semiconductor detection, especially suitable for the application scenarios of high voltage and high frequency wide band gap devices.

Keywords: β-Gao/SiC heterojunction; Multi-channel arbitrary wave signal synchronous measurement technology; Active voltage clamping technology; Wide band gap semiconductor detection1

1. Introduction

The development of semiconductor materials with wide band gap (WBG) and ultra-wide band gap (UWBG) poses a new challenge to device parameter measurement: these materials need to have high voltage tolerance, fast pulse response and high-precision waveform control, while traditional testing equipment has some limitations such as unstable amplitude-frequency characteristics in wide frequency domain and insufficient characterization of high-voltage nonlinear behavior, especially the characteristics of gallium oxide (Gao)/silicon carbide (SiC) and other materials highlight the adaptation defects of silicon-based platforms, so customized testing systems are urgently needed.

In this study, an innovative scheme is proposed: combining the characteristics of UWBG/WBG heterojunction transistor with active feedback control strategy to construct high-precision pulse and complex waveform generation technology. The core includes developing lateral β-Gao/SiC heterostructure adapted to high voltage environment, designing a measurement subsystem with real-time synchronous acquisition and dynamic adjustment of waveform parameters, optimizing switching performance and stabilizing output voltage by using heterojunction polarization effect, and breaking through the bandwidth limitation of traditional equipment.

2. Related work

In the field of semiconductor testing, high voltage pulse generation and arbitrary waveform synthesis technology have achieved breakthroughs through innovative paths. Traditional methods rely on Marx generator and linear amplifier to complete pulse shaping, but there are problems of limited frequency band and waveform distortion. With the development of wide band gap semiconductors, SiC and GaN devices have attracted attention due to their high voltage switching characteristics, but their integrated real-time waveform optimization platform is still in the early stage of research and development, and the application of ultra-wide band gap materials such as β-Gao is facing challenges.

The system designed in this study is based on heterojunction physics and real-time digital control technology to achieve a breakthrough, abandoning the independent modular architecture of waveform generation and correction, adopting a unified framework to integrate multiple functions, taking into account the material properties of switching devices and the requirements of high-precision signal synthesis. Compared with the prior art, it has obvious advantages in switching response rate, voltage regulation accuracy and frequency domain measurement accuracy.

3. Research on the hybrid method of generating high voltage pulse and arbitrary waveform

3.1. Design and manufacture of β-Gao/Sichfet

The transverse heterostructure combines the N-type β-Gao (100 nm) and P-type 4H-SiC (150 nm) layers grown by molecular beam epitaxy, and forms a two-dimensional electron gas (2DEG) channel at the interface, the carrier concentration of which is mainly determined by the polarization discontinuity between materials; n_s

$$n_s = \frac{\epsilon_0 \epsilon_r}{qd}(\Delta E_c - \Delta E_F) \tag{1}$$

Among them, the vacuum dielectric constant, the relative dielectric constant, the electron charge, the barrier thickness and the conduction band offset (1.8 eV) are optimized, and the breakdown voltage of heterostructure can exceed the design target of 800 V by using the improved field plate structure design. In the β-Gao material system, the critical electric field intensity reaches 8 MV/cm: $\epsilon_0 \epsilon_r q d \Delta E_c \Delta E_F V_{BR} E_c$

$$V_{BR} = E_c \cdot L_g \cdot \left(1 + \frac{\epsilon_{Ga_2O_3}}{\epsilon_{SiC}} \cdot \frac{t_{SiC}}{t_{Ga_2O_3}}\right) \tag{2}$$

When the gate length is fixed at 1μm, this parameter reflects the thickness of two-dimensional electron gas (2DEG) channel. Because the electron mobility in 2DEG reaches 180 cm2/v s, the on-resistance of the designed device can be kept below 5 mΩ cm2.

3.2. Design and implementation of digital programmable gate driver

The gate drive circuit adopts the digital-to-analog converter AD9106 with a resolution of 16bit and a sampling rate of up to 1 GS/s, and achieves precise synchronization control through the low jitter and high precision phase-locked loop LMK04828. The intrinsic nonlinearity of HFET can be compensated by using the gate voltage waveform in piecewise polynomial form: $V_g(t)$

$$V_g(t) = \sum_{k=0}^{3} a_k \left(\frac{t - t_0}{T}\right)^k \quad \text{for} \quad t \in [t_0, t_0 + T] \tag{3}$$

The coefficients are calculated in real time by Xilinx Versal ACAP FPGA based on transconductance Jacobi-

an matrix; a_k**J**

$$\mathbf{J} = \begin{bmatrix} \frac{\partial g_m}{\partial V_g} & \frac{\partial g_m}{\partial V_d} \\ \frac{\partial g_d}{\partial V_g} & \frac{\partial g_d}{\partial V_d} \end{bmatrix}^{-1} \tag{4}$$

Compared with the traditional linear driver, the adaptive predistortion technique can reduce the waveform distortion by 12dB.

3.3. Integrated closed-loop correction and active voltage clamping

The high-speed analog-to-digital converter ADC12DJ5200RF obtains the output signal with the help of the differential probe, and transmits it to FPGA through the signal conditioning module. Wiener filtering algorithm (Equation 5) is used to improve the amplitude-frequency characteristics. In order to suppress the fluctuation of the voltage peak during switching, the system adopts an active clamping circuit (formed by cascode SiCMOSFET) with dynamic adjustment ability, and updates the clamping voltage in time according to actual needs (Equation 6).

The feedback system selects ADC(ADC12DJ5200RF) with 14-bit sampling accuracy and 5GS/s sampling rate, and dynamically monitors the output signal with 10GHz differential probe, and adopts real-time Wiener filtering algorithm to improve the amplitude-frequency response; $H(\omega)$

$$H(\omega) = \frac{G^*(\omega)}{|G(\omega)|^2 + \Phi_n(\omega)/\Phi_s(\omega)} \tag{5}$$

The transfer function of the system is mainly determined by the noise and the power spectral density of the signal. In the active clamping circuit based on the cascode structure SiCMOSFET (model: C3M0065090D), the purpose of clamping can be achieved by dynamically changing the clamping voltage: $G(\omega)\Phi_n(\omega)\Phi_s(\omega)V_{clamp}$

$$V_{clamp} = V_{max} - \frac{I_{peak}}{g_{m,SiC}} \tag{6}$$

In the conversion period of 10ns, the overshoot suppression amplitude is less than 5%. This system has a flatness of ±0.5dB in the frequency range from DC to 100MHz.

4. Experimental results

4.1. Influence of switching characteristics on waveform generation fidelity

In order to verify the feasibility of the proposed method, a systematic experimental scheme was designed and implemented in this study, focusing on the switching characteristics, waveform generation accuracy and closed-loop calibration performance of heterojunction metal-oxide semiconductor field effect transistor (CHFET). The experimental platform includes high-frequency probe station, β-Gao/SICHF ET devices, gate drive circuit and high-precision measurement module, and each core component is designed with customized PCB to meet the technical requirements of parasitic inductance (less than 1nH).

In the design of pulse excitation source, the current-voltage conversion module of DA chip should be formed. Because the pulse signals fed back to DA chip through peak detection are all positive, its output must be able to generate negative voltage.

Switching characteristics: under the leakage current of 1μA, the breakdown voltage of the heterojunction transistor is 812V, and the on-resistance is low, which is 4.8mΩ·cm2. This characteristic accords with the theoretical value of Equation 2. The switching test with a 6GHZ bandwidth digital oscilloscope (Keysight

DSOX6034A) shows that the time of rising edge and falling edge is only 8.7ns at 0 V-600 V. Compared with the traditional SiC MOSFET, it is about 3.2 times higher. After adding the active voltage clamp circuit, the overshoot is effectively controlled, and the maximum value is 4.3% at the target voltage. This phenomenon also proves that the cascode active voltage clamp structure in Equation 6 does have technical advantages.

Which well confirms the stability and reliability of the system in the target bandwidth range.

4.2. Frequency response correction effect

The core principle of frequency domain correction is direct digital frequency synthesis technology DDS. DDS technology generates digital signal through phase accumulator and waveform memory, and then it is connected to amplitude-frequency correction network through digital-to-analog conversion to compensate parasitic effect. Without correction, the maximum amplitude fluctuation is ±3.2dB in the bandwidth of 100MHz, and the flatness is improved to ±0.48dB after using Wiener filter.

Frequency response correction: before and after Wiener filter correction, the amplitude-frequency characteristics of the closed-loop system are tested and analyzed in detail. Without correction, the amplitude-frequency response fluctuation of the system reaches ±3.2dB; in the bandwidth of 100MHz due to parasitic effects. After dynamic adjustment with real-time DSP algorithm (see Equation 5), this fluctuation is obviously reduced to ±0.48dB, which meets the technical requirements.which fully verifies the actual effect of the filter in improving signal fidelity.

Time-domain waveform distortion correction can be completed by using FIR filter. When the input signal x[n] passes through the N-order FIR filter (coefficients H[0]~H[N-1]), the high-frequency oscillation can be effectively suppressed and the amplitude deviation can be corrected, so that the rise/fall time of the output signal y[n] can be kept at about 10ns.

Thermal performance: Under the working condition of 600V/10A, the junction temperature of the heterojunction device is as high as 85℃, and its thermal gradient reaches 2.5℃/mm, which is much higher than the performance of similar SiC-based devices under the working condition of 150℃, mainly due to the very high thermal conductivity (~3.8 W/cm2.K) at the β-Ga2O3/SiC interface and the uniform Ga2O3 layer.

Which proves that the SiC integration scheme proposed in Formula (1) is obvious.

5. Future work

5.1. Future direction: Improve performance, scalability and integration

Technical improvement focuses on three aspects: first, the parasitic inductance is reduced to less than 60% and the switching time is shortened to 5ns through the integrated design of gate driving unit and HFET; Second, relying on the heterogeneous integrated Ga_2O_3/SiC photoelectric platform, tap the potential of performance improvement; The third is to improve the predistortion algorithm based on machine learning, replace the traditional polynomial correction, deal with the nonlinear memory effect in burst mode, suppress crosstalk and synchronize control in multi-channel architecture, or adopt the optical clock distribution scheme. Polarization effect study can adjust strain by controlling the gradient distribution of Al component in SiC layer, and improve the mobility of 2DEG. Using ternary β-(AlGa) O barrier material can dynamically adjust the threshold voltage, which provides the possibility for the optimization of high-voltage and high-frequency electronic devices and the development of new application scenarios.

6. Summarize

The heterojunction enhanced system proposed in this study has achieved a breakthrough in the field of semi-

conductor device testing, especially in the aspects of high voltage pulse generation and arbitrary waveform output. Based on the characteristics of β-Gao/SiC heterojunction, the architecture can realize fast switching below 10 nanoseconds at 800V, and the waveform accuracy can be ensured by real-time digital correction. Integrating adaptive gate drive and active voltage clamping technology, combined with Wiener filtering frequency response compensation strategy, the key technical problems of wide band gap devices are solved. Experiments show that the system is superior to the traditional scheme in switching speed, voltage load and signal integrity, and its scalability and thermal stability lay the foundation for the research and development of a new generation of semiconductor test equipment and power electronic systems. The research on monolithic integrated design and high-order predistortion algorithm is expected to expand its application scenarios and meet the needs of more complex waveforms.

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