Original Research Article

Research on the design and fabrication of GaNHemt devices with improved high-frequency performance

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Abstract: This study focuses on the design and manufacturing methods of GaN HEMT devices in terms of high-frequency performance improvement, and discusses the comprehensive testing, analysis, structural design, and optimization of the manufacturing process of the device. The static, dynamic and reliability tests and analysis of the performance of the device were carried out, and the material selection, epitaxial structure, gate and source-drain structure of the device were optimized to improve the effect of thermal management. The high-frequency performance and reliability of the device are further enhanced by means of epitaxial growth, device processing and packaging process optimization. This research provides key technical and theoretical support for the design and production of high-frequency GaN HEMT devices, with the main goal of promoting the efficient and stable application of GaN HEMT devices.

Keywords: GaN HEMT; High-frequency performance; Structural design

1. Introduction

GaN HEMT devices have broad development prospects in high-frequency and high-power applications due to their high electron mobility, wide bandgap and high breakdown voltage. However, enhancing its high-frequency performance and reliability remains a challenge. It is pointed out that the key to enhance the working characteristics of GaN HEMT devices is to optimize the material selection and epitaxial structure, reasonable design of gate and source-drain structure, and efficient thermal management. Targeted optimization of the fabrication process can further improve the electrical characteristics and reliability of the device. The purpose of this study is to systematically analyze the effects of the above factors on the performance of GaN HEMT devices and propose optimization solutions.

2. GaNHemt device performance testing and analysis

2.1. Static characteristic testing and analysis

As a basic part of the DC performance evaluation of GaN HEMT devices, the static characteristic test aims to obtain the key electrical parameters of the device during steady-state operation, such as threshold voltage, saturation drain current, drain on-resistance and breakdown voltage. During testing, measurements are typically performed using a parameter analyzer or a source measurement unit. The transfer characteristic test determines the threshold voltage by measuring the change in drain current by progressively adjusting the gate voltage (typically from -5 V to 3 V) at a fixed drain voltage (e.g., 10 V). For high-frequency GaN HEMT devices, the threshold voltage is generally 0~-3 V, and a low threshold voltage is conducive to improving the on-state performance and response speed of the device. The output characteristic test is plotted by measuring the change in drain current by gradually increasing the drain voltage (typically from 0 V to 50 V or higher) at a fixed gate

voltage (e.g., 0 V or -2 V). A typical GaN HEMT device should have a drain current of several hundred milliamps to several amperes in the saturation region (depending on the size of the device, depending on the design). In addition, the on-resistance (Rds(on)) between the drain and the source is determined. In general, GaN HEMT devices used in the mmWave band should have an Rds(on) of less than 1Ω, which reduces energy consumption and increases power gain. The breakdown voltage test of the device is a means to evaluate the withstand voltage of the device at high voltage, and is generally tested in the voltage range of 100 V and above, so as to ensure the stability and reliability of the device in high-power applications.

2.2. Dynamic characteristic testing and analysis

Dynamic characterization is essential to evaluate the performance of GaN HEMT devices in the high-frequency and microwave frequency bands. By measuring the S-parameter (scattering parameter), we can delve into key characteristics such as the gain of the device, the reflection coefficient of the input and output, the gain of the transmission, and its stability. Testing is typically performed using a vector network analyzer, such as Keysight's PNA-X Series, in the frequency range, which typically covers DC to 40 GHz or higher. In the specific test, the short circuit and open circuit calibration are carried out first to ensure the test accuracy. Then, S11 (input reflection coefficient), S21 (forward gain), S12 (reverse isolation), and S22 (output reflection coefficient) are measured at different frequency points. For high-frequency GaN HEMT devices, S21 typically has a larger gain than frequency and decreases as the frequency increases, with cut-off frequencies typically ranging from tens of GHz to 100 GHz or higher. Typical dynamic characterization test results show that the S21 should maintain a gain of 15-20 dB or higher below 10 GHz and 10 dB or higher at 40 GHz to ensure its application performance in the mmWave band. Measurements of the noise figure and linearity of the device are also required for high-frequency applications. The noise figure test is to calculate the noise figure by applying a known power signal source to the input terminal, and measuring the signal power and noise power at the output terminal. Generally, the noise figure of GaN HEMT devices is required to be less than 1~2 dB to meet the needs of low noise amplifiers.

2.3. Reliability testing and analysis

GaN HEMT device reliability testing is critical to ensure stable performance of devices under long-term operation and extreme operating conditions. Reliability testing typically covers a variety of test methods, including high-temperature operating life (HTOL) testing, power cycling testing, and voltage acceleration testing. The purpose of HTOL testing is to evaluate the long-term stability of the device in a high-temperature environment, which is generally tested in an environment with an ambient temperature of 150°C and above, plus rated drain current and voltage, and the test time is up to several thousand hours. This test can reveal the effects of device aging at high temperatures, such as reduced mobility, threshold voltage drift, and increased leakage current. The power cycling test is used to evaluate the thermal stability and reliability of the device during repeated power on and off cycles. During the test, the device repeatedly switches between high and low power states to simulate a real-world operating thermal shock environment. Typical test conditions include applying more than 100 W of power and more than 10,000 cycles. This test helps to determine the reliability of gate metal migration and surface crack generation due to thermal fatigue.

3. Improve the structure design of GaN HEMT devices with high-frequency performance

3.1. Material selection and epitaxial structure optimization

In order to achieve the best performance in high-frequency applications, it is necessary to select materials with excellent electrical and thermal properties, and achieve high electron mobility and good current transmission through the fine design of the epitaxial layer. Generally speaking, the materials used in GaN HEMT devices include GaN, AlGaN, and AlN, among which GaN, as the main material, can provide high electron mobility and breakdown voltage; AlGaN is used as a barrier layer, and its main function is to generate two-dimensional electron gas (2DEG) at the interface. The thin layer design of AlN can enhance the stress at the interface, thereby increasing the concentration and migration rate of 2DEG. In addition, low-defect density semi-insulating SiC or Si substrates are usually used for epitaxial growth to reduce thermal resistance and improve heat dissipation. In the process of optimizing the epitaxial structure, it is often necessary to precisely control the thickness of the AlGaN barrier layer and the concentration of the Al component, as this has a direct impact on the concentration and migration rate of 2DEG. In high-frequency applications, the thickness of the barrier layer is usually in the range of 10-30 nm, while the concentration of the Al component is generally maintained in the range of 25%-30% to ensure a high electron density and low electrical resistance. In addition, the introduction of buffer layers (e.g., AlN or GaN buffers) to suppress dislocations caused by lattice mismatch should be considered, thereby improving the crystal quality and electrical properties of the material. In the application of ultra-high frequency, it is found that the use of a gradient AlGaN barrier layer with gradient Al components can reduce the influence of polarized electric field at the interface, thereby further enhancing the electron migration ability of 2DEG.

3.2. Gate and source-drain structure design

Optimized design of gate and source-drain structures in GaN HEMT devices to enhance high-frequency performance is key. The gate design has a direct impact on the main parameters of the device, such as gain, cut-off frequency, and power density. In order to speed up the response of the device at high frequencies, a T- or Ω-type gate design is often chosen, which can significantly reduce the length of the gate, usually no more than 0.2 μm, and in some cases, the size can reach 0.05 μm, which helps to reduce the resistance and capacitance of the gate, thereby significantly enhancing the performance of the device at high frequencies. In addition, the choice of gate material is crucial. The gate materials commonly used are titanium, aluminum, and nickel, which have small work functions and good adhesion, which is conducive to the formation of stable Schottky contacts and ensures stable and reliable high-frequency operation. The source-drain structure design has the same effect on the high-frequency characteristics of the device. In order to reduce the effect of parasitic resistance and parasitic inductance, a large area of heavily doped n+GaN contact layer is usually chosen as the source leakage electrode, while ensuring that the contact resistance does not exceed 0.1Ω ··. In addition, optimizing the arrangement of the source-leakage electrode and the multi-finger electrode structure can significantly reduce the parasitic effect and increase the current density. In order to more effectively reduce the capacitance and inductance between sources and drains, and to enhance their high-frequency response, we can consider using a short source-drain spacing, which is typically designed in the range of 1-3 μm, which maximizes open-state conduction performance and gain.

3.3. Thermal management design

Due to the operation of high-frequency and high-power conditions, a large amount of heat is generated in GaN HEMT devices, so how to effectively manage and dissipate heat is directly related to their reliability and long-term stability. First of all, when selecting substrate materials, priority should be given to materials with higher thermal conductivity, such as semi-insulating SiC substrates, which can achieve a thermal conductivity of 490 W/mK, which is significantly higher than that of conventional silicon substrates (150 W/mK). This solution significantly reduces thermal resistance and heat conduction efficiency. In addition, during epitaxial growth, a thinner GaN buffer layer can be used to reduce heat accumulation, and a low thermal resistance interface layer (e.g., AlN) can be added between the substrate and the epitaxial layer to improve the thermal diffusion capacity. In the design of the device structure, the backside heat dissipation technology can be introduced, which further improves the heat dissipation efficiency by plating a layer of high thermal conductivity material (such as copper or gold) on the back of the device and adding a heat sink or heat pipe structure to it. It is found that this special backside heat dissipation design can reduce the junction temperature of the device by more than 30%, thereby enhancing the stability of the device in high-frequency environments. Thermal management can also be improved by optimizing the device layout design, such as spacing multiple high-power devices to increase the surface area of the hot runner and heat dissipation and reduce the formation of local hot spots.

4. Optimize the fabrication process of GaNHemt devices to improve high-frequency performance

4.1. Optimization of epitaxial growth process

In order to achieve high electron mobility and low leakage current in high-frequency applications, the quality and interface properties of the materials need to be strictly controlled during epitaxial growth. In the growth of GaN and AlGaN layers, metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy are commonly used. In the MOCVD process, by accurately adjusting the flow ratio and reaction temperature of ammonia and metal-organic sources (such as trimethylgallium, TMGa), the present invention can effectively regulate the composition and thickness of GaN, AlGaN layer, and the general growth temperature is 1050-1100 °C, which ensures the crystal quality of the material and improves the electron mobility. Further introduction of growth interruption or stepped temperature annealing can reduce the dislocation density of the epitaxial layer, improve the interface flatness, and enhance the electron transport performance. In order to further enhance the performance of the device at high frequencies, we can consider adding a specific insertion layer or superlattice design to the AlGaN/GaN interface, such as the AlN insertion layer or the AlGaN/GaN superlattice, by increasing the concentration and migration rate of the two-dimensional electron gas (2DEG), we can better optimize the charge distribution at the interface. Studies have shown that these insertion layers need to be tightly controlled in thickness and period to the nanometer level in order to balance electron concentration and mobility. In addition, in order to reduce the introduction of impurities and the formation of defects, the pretreatment steps of epitaxial growth can be optimized, in which hydrogen plasma scrubbing and low-temperature GaN buffer layer growth can be used to reduce interfacial contamination and improve lattice matching. Further optimization of the epitaxial growth process also includes the use of advanced reactor design and flow field control technology to ensure uniform gas distribution and reduce impurity deposition.

4.2. Device processing process optimization

Optimizing the device processing process is key to enhancing the high-frequency performance of GaN HEMT devices. In order to maximize the high-frequency response, the distance between the gate length and the source-drain electrode must be accurately controlled to reduce parasitic capacitance and parasitic inductance. Electron beam lithography is commonly used to achieve patterned designs of submicron and even nanometer gates. By adjusting the exposure dose, increasing the voltage, and optimizing the development process, we were able to obtain a gate structure with high resolution and low damage. Dry etching techniques such as Reactive Ion Etching (RIE) are then used to transfer patterns across the gate region to ensure the steepness and uniformity of the gate edge and reduce the effects of parasitic effects. In order to further optimize the device processing process, the metal deposition process is also of great significance. Using electron beam evaporation or magnetron sputtering, the gate, source-leakage electrode thickness and its uniformity can be accurately controlled. In the fabrication of source-leakage electrodes, multiple layers of metal (e.g., Ti/Al/Ni/Au) are often required and rapidly thermally annealed to create a low-resistance ohmic contact. Optimizing annealing conditions, such as choosing the right temperature and time, should significantly reduce the contact resistance to less than 0.1 Ω ·· mm, thereby enhancing the density of the current and the conductive properties at turn-on.

4.3. Packaging process optimization

In high-frequency applications, the design of the package structure needs to take into account the requirements of electromagnetic compatibility and thermal management. In order to reduce parasitic inductance and parasitic capacitance, coplanar packages (e.g., die flip wire, chip package, etc.) are often used to minimize the length of the electrical interconnect, while introducing low-loss lead materials (such as gold or copper wires) and high-thermal conductivity package substrates (such as aluminum nitride AlN or silicon nitride Si3N4) to ensure the transmission integrity and efficiency of high-frequency signals. At the packaging stage, we can use cutting-edge flip chip technology to mount GaN HEMT chips directly on a highly thermally conductive substrate, such as a copper substrate or aluminum nitride substrate, which can significantly reduce thermal resistance and thus improve heat dissipation efficiency. In addition, by adopting microelectromechanical systems (MEMS) technology, we are able to achieve a more compact package design, which not only further reduces the parasitic effects of the device, but also improves the efficiency of its thermal management. The optimized packaging process further comprises: adopting conductive silver paste or high thermal conductivity adhesive as thermal conductive material to ensure efficient heat conduction between chip and packaging substrate. In order to improve the heat dissipation performance of the package, the integrated heat sink or copper chip packaging technology can also be applied to the chip, which is directly connected to the back or side of the chip through the heat sink to efficiently and quickly dissipate heat to the outside. Studies have shown that the use of multilayer ceramic packaging technology (such as low-temperature co-fired ceramic LTCC) can significantly reduce the package inductance and improve high-frequency performance. At the same time, the selection of sealing materials is an optimization focus when encapsulation, and low-dielectric constant and low-loss factor packaging materials such as polyimide or epoxy resin should be used to reduce signal attenuation and parasitic effects.

5. Conclusion

In this study, the performance test, structural design and preparation process of GaN HEMT device were

systematically optimized, in order to provide comprehensive theoretical and technical support for enhancing the high-frequency performance of the device. Future research should further explore more efficient material systems and finer process control to promote the real development of GaN HEMT devices in the direction of higher frequency and power applications.

About the author

Pengbo Liu (2000-), male, was born in Nanjing, Jiangsu Province, China, student, research direction:Gallium nitride microwave amplifier chip design and process implementation

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