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Original Research Article

Research on the dome angle of polysilicon gate

Yili Xu[1], LI Xin[1], Xiaodong Yin[1], Guowei Zhang[1], Jingyi LI[1], Qianqian Liu[2]

1 Hangzhou Spectrum Semiconductor Co., Ltd., Hangzhou Xiaoshan, 310000, China
2 Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, 100029, China

Abstract: In this paper puts forward a kind of polysilicon gate dome Angle manufacturing method, the polysilicon gate top Angle etching corners, avoid the silicon carbide MOSFET switch process, the polysilicon gate top electric field concentration, successfully solved the current silicon carbide power MOSFET industry in the polycrystalline top Angle of reliability problems and hidden trouble. This method is simple, effective, feasible and has obvious advantages, with high process tolerance, which can provide guarantee for the products working under extreme conditions.

Keywords: Silicon carbide MOSFET; Polysilicon; Dome Angle; Reliability

1. Introduction

With the rapid development of semiconductors, polysilicon materials have been widely used in the fields of solar cells, integrated circuits and photoelectric devices because of their excellent physical and chemical properties[1,2,3]. In the current field of power semiconductor, VDMOSFET devices made with silicon carbide substrate and epitaxial component have become one of the mainstream. For VDMOWFET devices, because their electrode structure is mostly above the epitaxial layer, how to minimize the thinning of each membrane layer while meeting the reliability requirements of the basic device has become the key to improve the reliability of the devices. The schematic diagram of the cell structures of the existing VDMOSFET devices is shown in **Figure 1**

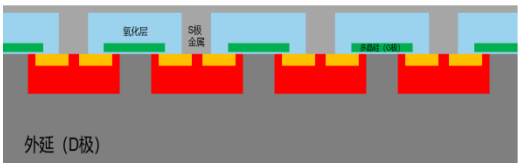

Figure 1. Schematic diagram of the cell structure of the existing VDMOSFET devices.

As shown in Figure 1, G is extremely polysilicon, and the oxide layer separates the G pole and the S pole. How to improve the electric field bearing capacity of the oxide layer as far as possible under the certain quality of the oxide layer has become a key point to improve the reliability of the device. When the device works, it is necessary to apply a forward voltage to the polysilicon gate. Because the gate and the source, there is a potential difference, and the electric field in the oxide layer will be concentrated at the sharp corner of the polysilicon gate. The concentration of the electric field will cause the oxidation layer to be easily broken down[4,5,6], Reduce the reliability of the devices[7,8].

In this paper, an etching method of circular polysilicon top Angle is proposed. Using the defect etching method of U groove etching subtrench (mainly the etching defects produced by high power and high selection ratio) + the supplementary method of silicon oxide, the process scheme is improved to solve the problem of electric field concentration.

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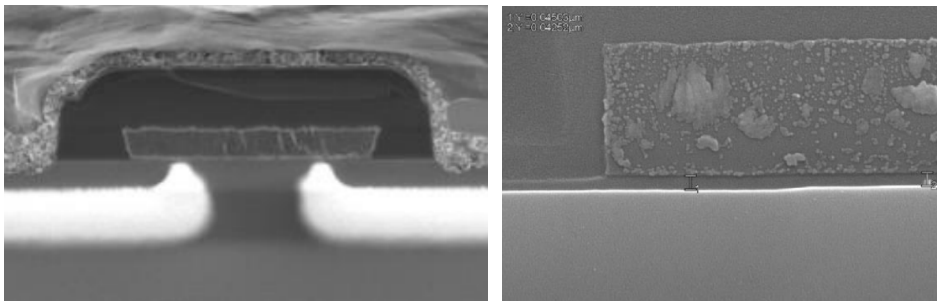
2. The polysilicon gate morphology in the international market and the solutions of each device manufacturer

The top Angle of the polysilicon gate is mainly because the manufacturing of the polysilicon gate needs to use the anisotropic method of dry etching. This etching will make the etching rate different in different directions, and this difference will lead to the morphology of the polysilicon etching often with a sharp top Angle[9,10].

It is difficult for various manufacturers in the industry to eliminate the sharpness of the polycrystalline top Angle in terms of process. As shown in Figure 2, the cell cross section map after the dissection of the current commonly used SiC MOSFET products on the market. All the polysilicon has sharp angles from the figure. Therefore, there are two main ways to prevent the breakdown of the current industry: 1, increase the thickness of the oxide layer of the isolation medium; 2, silicon oxide supplement method.



(a) (b)

Figure 2. Cell cross-section diagram of the silicon carbide device.

Figure 1. Cross-sectional view of the unit cell of a silicon carbide device.

2.1. Increase the thickness of the isolation oxide layer

Increasing the thickness of the isolation oxide layer is to increase the thickness of the isolation oxide layer, so that the electric field strength in the isolation layer of the device is a palliative but not the root cause, which is a helpless move. However, the increase of the thickness of the isolation layer brings new problems to the device:

First, the thicker isolation layer represents a greater stress when the device faces changes at high and low temperatures. Because the thermal expansion coefficient of the material is fixed, the doubling of the thickness means that the expansion size of the material is doubled when the temperature increases, and the stress generated by the expansion of the materials will be concentrated at the sharp Angle, which will cause a significant burden and serious negative impact on the reliability of the device;

Secondly, because silicon carbide devices are mostly used in the field of high frequency, the polysilicon gate will constantly be charged and discharged in the work, the charge repeatedly gathered at the sharp corner, the accelerator aging, greatly reduce the life of the device.

Therefore, increasing the thickness of the isolated oxide layer is not a good solution.

2.2. Silicon oxide supplement method

The general process and effect of the silicon oxide supplement method are shown in Figure 3. First, grow the polysilicon on the wafer; second, lithography, etching the polysilicon; then, the growing silicon oxide completely covers the remaining polysilicon; then the whole silicon oxide is etched, leaving the polycrystalline and silicon oxide side walls; finally, the silicon oxide is deposited again, used as the isolation medium layer.

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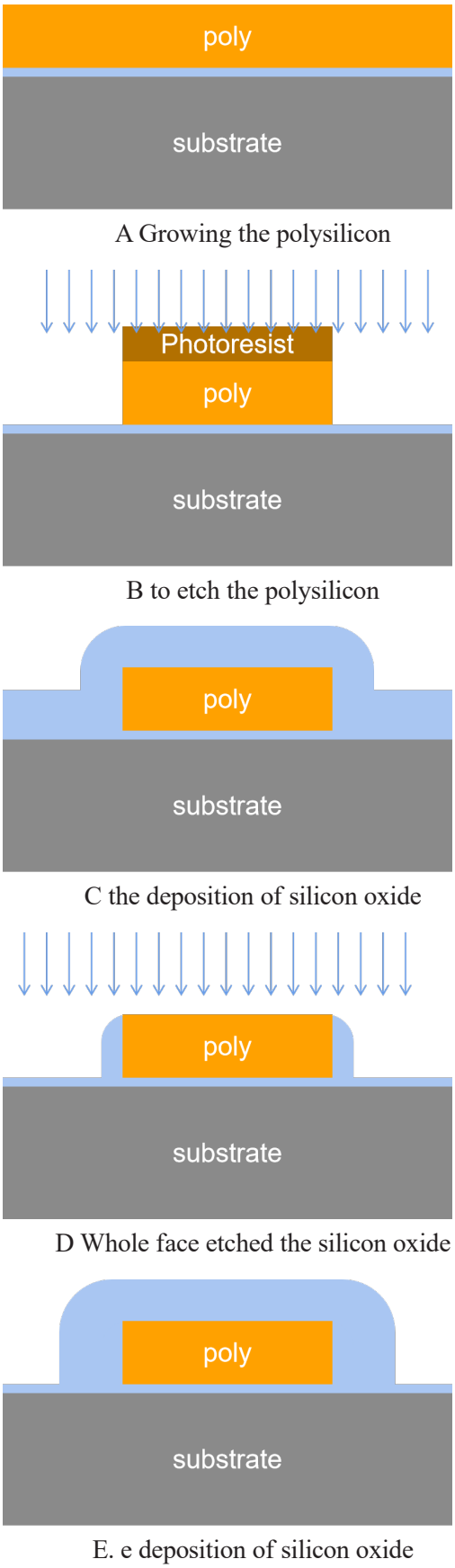

Figure 3. General process and effect of the silicon oxide supplement method.

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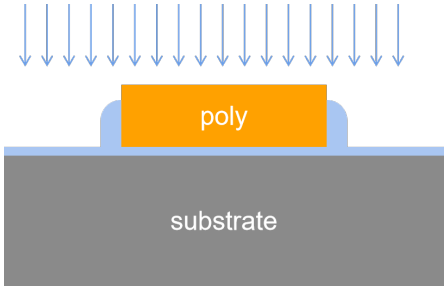
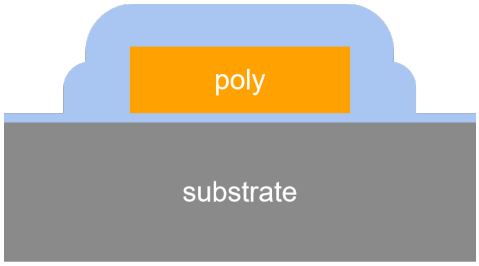
This method reduces the risk of gate source breakdown by increasing the lateral thickness of the silicon oxide side wall, increasing the oxide layer and reducing the sharpness of the oxide layer after the oxide layer deposition, but it does not fundamentally solve the problem of electric field concentration caused by the polysilicon tip Angle. As shown in Figure 4, a slight deviation in the etching of the oxide layer results in poor results.



A Whole deviation of silicon oxide

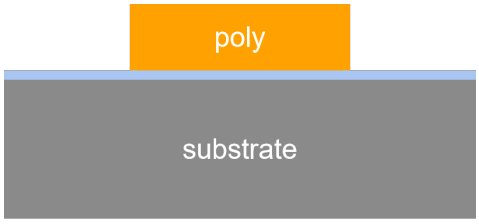


B to cause the actual results

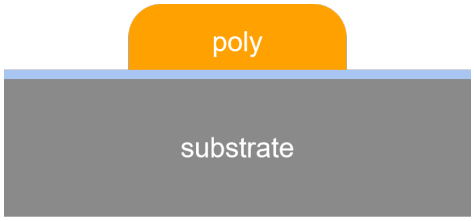
Figure 4. Schematic diagram of the actual results of the silicon oxide supplement method.

3. The etching method of circular polycrystalline top angle

This paper proposes a new etching method, which can etch the polysilicon to form a rounded top Angle, fundamentally solve the problem of electric field concentration, improve the device reliability, and change the comparison diagram before and after as shown in Figure 5.



A The existing polycrystalline post-etching morphology



B Polycrystalline morphology after etching of the method described in this paper

Figure 5. Comparison of the processing before and after the etching method of the circular polycrystalline top angle.

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3.1. Process flow

The process methods and processes adopted are as follows:

1. To deposit a layer of polysilicon on the epitaxial wafer surface using the LP-CVD equipment.

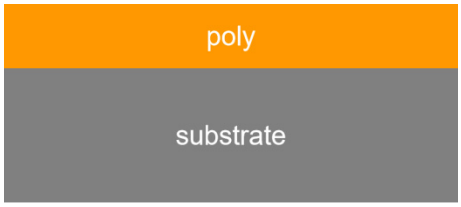

Figure 6. Deposition of polysilicon.

2. Pre-baking, glue, exposure, development, fixation, forming the pattern.

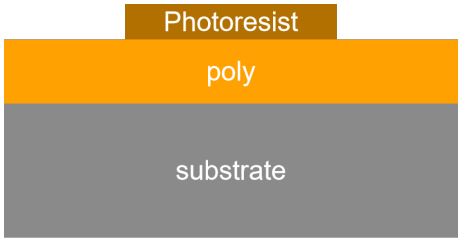

Figure 7. Lithography.

3. Anisotropically etched the polysilicon to remove the photoresist.

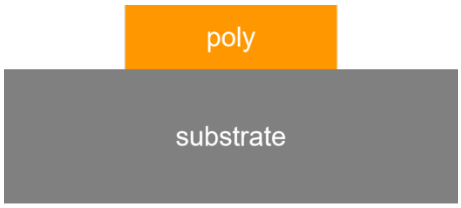

Figure 8. Etching, deglue removal.

4. The silicon oxide medium was deposited with LP-CVD.

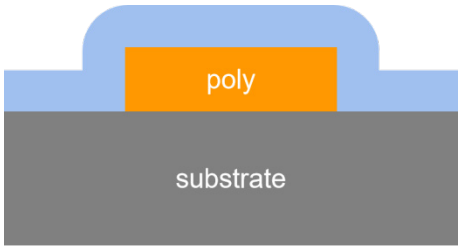

Figure 9.

5. The anisotropic whole surface is etched with silicon oxide to form a side wall.

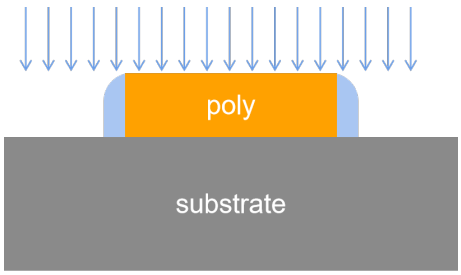

Figure 10. Whole-face etching.

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6. Using high power, high selection than the etching method of etching polysilicon.

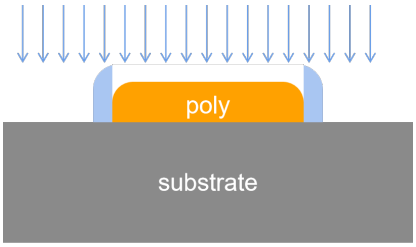

Figure 11. Etched polysilicon.

7. Remove the oxide layer side walls.

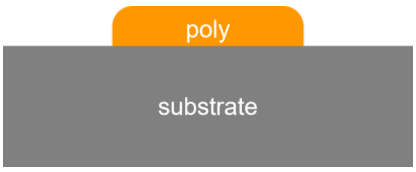

Figure 12. Removal of the side walls

8. Dimedium oxide layer.

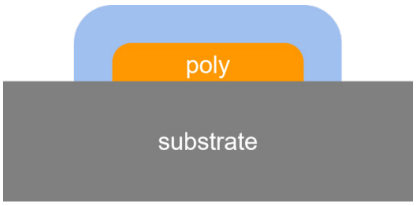

Figure 13. Deposited the oxide layer.

The actual result profile of VDMOSFET device produced by the present method is shown in Figure 14.

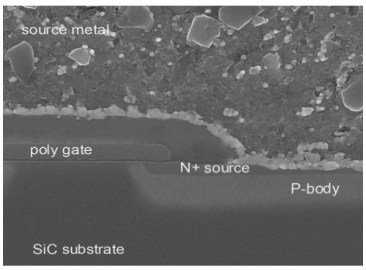

Figure 14. Profile of the method.

3.2. Advantages and benefits

The etching method used in this paper has the following advantages and benefits:

1. The etching method described in this paper is relatively simple and does not require repeated lithography; this greatly reduces the process requirements and saves a lot of time;

2. The etching method described in this paper can directly change the top Angle of polysilicon to rounded corners; this will fundamentally solve the problem of electric field concentration, and reduce the concentrated release of the stress and improve the reliability of the device;

3. This method has a high process tolerance, even if the process conditions appear large deviation, the final sample can achieve the ideal appearance.

4. Conclusion

The etching method of circular polycrystalline top Angle proposed in this paper has obvious advantages compared with the existing technology:

1. The top Angle of polysilicon into a round Angle, fundamentally solved the problem of electric field concentration;

2. Benefiting from advantage 1, the thickness of the isolation layer of the device will be greatly reduced;

3. Benefit from the advantage of 2, the reliability of the device will be greatly improved;

4. With a higher process tolerance, even if there is a large deviation in the process, it will not have a large impact on the results, let alone cause the results similar to those shown in Figure 4.

To sum up, the "etching method of circular polycrystalline top angle" proposed in this paper has a significant contribution to the reliability of silicon carbide power MOSFET devices, especially can increase the high and low temperature impact resistance of the devices, which will provide process guarantee for the reliability of the devices working under extreme conditions.

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