Original Research Article

Chip design requirements for building a comprehensive low altitude flight safety protection system

Feifei Zhang; Linying Cai

Hangzhou Shengyuan Data Security Technology Co., Ltd., Hangzhou, Zhejiang, 311121, China

Abstract: With the rapid advancement of drone and low altitude aircraft technology, it is particularly important to establish a comprehensive low altitude flight safety guarantee system. The article focuses on the key requirements of chip design in this context, aiming to improve the safety, reliability, and efficiency of flight. Firstly, the current technological challenges were analyzed, including high-precision positioning and navigation, real-time data processing capabilities, low energy consumption, and security guarantees. To address these issues, requirements are proposed in terms of hardware to improve integration, optimize signal processing units, and power management strategies; At the software level, the importance of developing lightweight operating systems and optimizing algorithms is emphasized. By comprehensively considering these factors, specific suggestions are provided for the design of low altitude aircraft chips, aiming to promote the industry's development towards a safer and more efficient direction.

Keywords: Low altitude flight; Security protection; Chip design requirements

1. Introduction

In recent years, drones and other low altitude aircraft have shown great potential in fields such as logistics distribution, agricultural monitoring, and disaster relief. With its widespread application, safety hazards have gradually emerged, such as frequent incidents of aircraft loss of control and collisions, posing a threat to safety. Building an efficient and reliable low altitude flight safety guarantee system has become an urgent task. In this system, the chip serves as a key component, and its design level directly affects the overall performance of the system. High quality chip design can not only improve the stability and safety of aircraft, but also enhance their ability to cope with complex environments, effectively reducing the possibility of accidents and ensuring the safe conduct of low altitude flight activities. Optimizing chip design is of great significance for promoting the healthy development of the entire industry.

2. Key technical challenges

2.1. High precision positioning and navigation

To ensure precise positioning of low altitude aircraft in complex environments, the chip should support multiple Global Navigation Satellite Systems (GNSS), including GPS, GLONASS, Galileo, and BeiDou. By integrating these systems, the chip can provide a wide coverage range and higher positioning accuracy. Research shows that in complex environments such as urban canyons or dense forests, the positioning error of a single GNSS can reach tens of meters, while multi system collaboration can reduce the error to sub meters. The multi band signal processing capability further enhances the anti-interference performance of the chip, ensuring stable and reliable data transmission. This precise positioning not only improves the accuracy of autonomous navigation for aircraft, but also optimizes the response speed and accuracy of obstacle avoidance systems, thereby significantly enhancing the safety and efficiency of low altitude flight. By utilizing the characteristics of different GNSS systems, even in extremely challenging environments, aircraft can still achieve precise position perception, ensuring their safe and stable operation.

2.2. Real time data processing capability

Chip design should have the ability to efficiently process multiple sensor data, achieving real-time perception and rapid response to the surrounding environment. The data sources involved include cameras, radar, and ultrasonic sensors. In drone operations, the amount of data generated per second can reach hundreds of megabytes, and processing this information quickly and accurately is crucial for avoiding collisions. By adopting advanced signal processing algorithms, the chip can parse input data in milliseconds, ensuring that the aircraft can recognize and avoid obstacles in real time. The optimized hardware architecture supports multitasking parallel processing, significantly improving system efficiency. According to research, chips integrated with high-performance processors can increase the success rate of low altitude aircraft in complex environments by about 30%. This capability not only enhances the safety of the aircraft, but also broadens its application scenarios, enabling it to maintain stable operation in diverse environments. By integrating data from different sensors, the chip provides a solid technical support for low altitude flight.

2.3. Low power design

Given that low altitude aircraft rely on battery power, reducing energy consumption has become the key to extending their endurance. Research shows that optimizing chip design and algorithm efficiency can significantly reduce power consumption. For example, advanced power management technologies such as Dynamic Voltage and Frequency Regulation (DVFS) are used to adjust power consumption in real-time according to computing needs, saving up to 30% of energy. The efficient hardware architecture further reduces non essential energy consumption, making energy utilization more intensive. In practical applications, such energy-saving measures have increased the average endurance time of aircraft from 45 minutes to over 60 minutes. Meanwhile, the optimized chip supports multi-sensor data processing while maintaining performance, enhancing flight safety and stability, and extending working hours. By comprehensively utilizing various energy-saving strategies, the endurance of the aircraft has been effectively improved without increasing battery capacity, greatly enhancing its operational flexibility and task execution efficiency. This provides a broader development space for the application of low altitude aircraft.

2.4. Safety and reliability

Chip design needs to integrate security mechanisms to resist malicious attacks and flight accidents caused by malfunctions, and ensure stable operation under extreme conditions. Research has shown that the risk of network attacks on low altitude aircraft is increasing year by year, with approximately 20% of security incidents stemming from hardware vulnerabilities. For this purpose, the chip should be equipped with an encryption engine and secure boot function to prevent unauthorized access and data tampering. Meanwhile, adopting fault-tolerant design and redundancy mechanism can effectively deal with hardware failures and improve system stability. For example, the implementation of the third mock examination Redundancy (TMR) technology can improve the reliability of key components to 99.99%, significantly reducing the risk of system failure caused by a single point of failure. In response to extreme environments such as sudden temperature changes, high humidity, and strong radiation, the chip needs to undergo rigorous testing to ensure its normal operation within the range of -40 ° C to 85 ° C. This comprehensive security protection not only ensures the physical safety of the aircraft, but also enhances the reliability of data transmission, providing solid technical support for low altitude flight. This enables the aircraft to maintain efficient and stable operation in complex and ever-changing environments.

3. Chip design requirements

3.1. Hardware level

3.1.1. Integration degree

Improving chip integration can significantly reduce circuit board area, lower overall weight, and enhance the maneuverability and endurance of aircraft. By adopting System in Package (SiP) technology, multiple functional components can be integrated into a single chip, reducing circuit board area by about 40% and equipment weight by up to 30%. Compact design not only optimizes space utilization, but also reduces the energy required to maintain flight due to lightweight design. In addition, high integration shortens the signal transmission distance, accelerates data processing speed, and improves system response efficiency and reliability. In high-performance drone applications, this chip can increase endurance by 25% and support more agile maneuverability, which is crucial for executing complex tasks. Optimizing chip integration is crucial for improving the performance of low altitude aircraft, providing technical support for efficient and flexible task execution, enabling the aircraft to perform well in various environments.

3.1.2. Signal processing unit

It is necessary to design specialized data accelerators to meet the real-time processing needs of low altitude aircraft for sensor data. This accelerator can efficiently process massive amounts of data from various sensors such as cameras, radar, and ultrasonic sensors. Research has shown that in drone operations, up to several hundred megabytes of data can be generated per second. Traditional general-purpose processors are difficult to process this data in a timely manner without affecting system performance, while dedicated accelerators can significantly improve processing speed by optimizing algorithms and hardware architecture. For example, by using customized hardware accelerators, data processing latency can be reduced from tens of milliseconds to a few milliseconds, greatly improving response speed. Secondly, this accelerator supports parallel computing, making simultaneous processing of multi-sensor data more efficient. According to experimental data, using a dedicated accelerator can increase the overall computational efficiency of the system by about 50%, while reducing power consumption by up to 30%. This not only enhances the safety and stability of the aircraft, but also expands its application scenarios, enabling it to perform more precise tasks in complex environments. By integrating high-performance accelerators, low altitude aircraft can achieve precise navigation and obstacle avoidance in rapidly changing environments, ensuring successful mission execution.

3.1.3. Power management

Implementing advanced power management strategies is crucial for optimizing the energy efficiency of low altitude aircraft. By adopting technologies such as dynamic voltage and frequency regulation (DVFS), task scheduling optimization, and intelligent sleep mode, the efficiency of battery usage can be significantly improved. Research has shown that DVFS technology can adjust the power supply voltage and frequency in real-time according to the workload of the processor, saving up to 30% of energy consumption without affecting performance. Meanwhile, optimized task scheduling algorithms can ensure reasonable allocation of resources during high load periods and avoid unnecessary energy waste. For example, the intelligent sleep mode can automatically shut down some circuits when the aircraft is in an inactive state, reducing static energy consumption. Experimental data shows that this can save an additional 20% of energy. By combining these strategies, the overall energy utilization rate can be increased by about 40%, effectively extending the endurance of the aircraft. In practical applications, this comprehensive power management solution has increased the average endurance time of some drones from 45 minutes to over 60 minutes. By precisely controlling and optimizing the energy consumption of each component, not only has the aircraft's continuous operational capability been enhanced, but its operational flexibility and task execution efficiency have also been improved. These improvements provide stronger competitiveness and technical support for low altitude aircraft in a wider range of application scenarios.

3.2. Software level

3.2.1. Operating system

Developing a lightweight operating system (OS) suitable for embedded systems is crucial for supporting multi task parallel execution of low altitude aircraft without affecting system performance. An ideal lightweight operating system needs to have efficient task scheduling mechanisms, optimized memory management, and real-time response capabilities. Research has shown that operating systems designed with a streamlined kernel can shorten startup time to less than 100 milliseconds and reduce memory usage by approximately 60%. This not only improves response speed but also frees up more resources for critical applications. For example, lightweight operating systems such as Zephyr and FreeRTOS have demonstrated superior performance in resource constrained environments. These systems ensure timely processing of high priority tasks and guarantee real-time performance through priority scheduling algorithms. Experimental data shows that when running multiple sensor data processing tasks, the overall delay can be controlled within a few milliseconds, which is nearly 50% faster than the response speed of traditional systems.

3.2.2. Algorithm optimization

Optimize algorithms for specific application scenarios of low altitude aircraft, such as path planning and obstacle avoidance algorithms, to ensure that the decision-making process is both fast and accurate. In the field of path planning, although the A * algorithm is classic, it has high computational complexity when facing large-scale environments. The Theta * algorithm is adopted as a heuristic improved version of A *, which reduces the search space and improves efficiency by relaxing the requirement for direct visibility between nodes. Experiments have shown that Theta * can reduce computation time by about 40% compared to traditional A * algorithms in complex environments. For obstacle avoidance algorithms, artificial potential field method is a common strategy, but it is prone to getting stuck in local minimum problems. By combining genetic algorithm (GA) with artificial potential field method, GA's global search capability is utilized to optimize potential field parameters, effectively avoiding local optima. Research has shown that this combination method increases the obstacle avoidance success rate to 95%, which is 25 percentage points higher than using the artificial potential field method alone(See **Figure 1**).

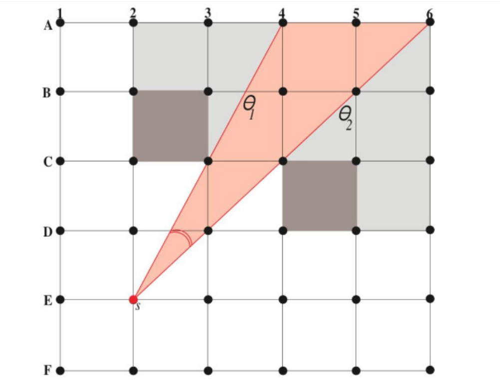

Figure 1. Schematic diagram of Theta * algorithm.

The Fast Random Tree (RRT) algorithm provides a solution for real-time obstacle avoidance in dynamic environments. The introduction of Bi directional RRT not only maintains the original advantages, but also significantly accelerates the exploration speed. The test results show that compared to unidirectional RRT, Bi directional RRT can explore more feasible paths at the same time, with an average path length reduction of 25%. By improving existing algorithms, integrating multiple algorithms, and adjusting parameter configurations, the quality of task execution decisions and response speed of low altitude aircraft can be significantly optimized. For example, using Theta * to optimize path planning, combining GA and artificial potential field methods to solve obstacle avoidance problems, and applying Bi directional RRT to enhance exploration efficiency in dynamic environments. The application of these technologies provides solid technical support for dealing with complex and ever-changing task environments.

4. Conclusion

In short, building a comprehensive low altitude flight safety protection system requires attention to chip design and development, not only to overcome technical challenges, but also to consider cost-effectiveness. Future research should focus on improving the functionality and adaptability of chips to better meet the development needs of low altitude flight. By optimizing the design, we ensure that the chip achieves the optimal balance between performance, energy consumption, and security, thereby promoting progress and innovation in the entire industry. This provides key technical support for achieving safer and more efficient low altitude flight operations.

About the author

Zhang Feifei (1982.5-), male, Han, from Luoyang, Henan, holds a master's degree and is an associate researcher. His research direction is image processing chip design.

References

[1] Luo Xin, Feng Wu, Sun Weijie Design and Implementation of Signal Processing Control Platform for Low altitude Warning Radar [J]. Modern Radar, 2023 (2): 75-80

[2] Yu Guang, Luo Liquan, Wu Tong, etc Design of High Reliability Switching Power Supply with Low Altitude Light Load Loss [J]. Electronic Design Engineering, 2021 (19): 88-92

[3] Ma Zhenghua, Sun Bin Design of Short Distance Low Altitude Transportation System Based on Four Axis Aircraft [J]. Computer Measurement and Control, 2016 (10): 205-208